INTEGRAL UNIVERSITY, LUCKNOW
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

COURSE: ASIC DESIGN & FPGA
COURSE CODE: EC508
COURSE CREDIT: 4

PREREQUISITES:

Subject	Description	Level of study
-	-	-

COURSE OBJECTIVES:

- To understand the concepts of design issue in system development, Architecture of 8051 µc and its description, Pin diagram of 8051 µc and its description, addressing modes, instruction sets, Arithmetic and logical operation, Sub-router, Interrupt handling timing sub-router, Serial data transmission, Serial data communication.
- To understand Types of ASIC, ASIC cell library, CMOS logic, CMOS Process, CMOS Design rule, Combinational logics, Combinational logics, Data path logic cell, Sequential logic cell, I/O cell, cell compiler.
- To understand the mechanism of ASIC library cell design: Transistor and resistors, Transistor parasitic capacitance, Logical Effort, Library cell design, Library architecture, Gate array design, standard cell design, Programmable ASIC Design, Anti fuse, Static RAM, EPROM, EEPROM Technology
- To understand Low level Design Entry, Schematic design Entry, Language, PLA, Tool, EDIF, Overview, Hardware descriptive language VHDL, Hardware descriptive language Verilog, Logic synthesis VHDL Simulation, Logic synthesis VHDL Simulation, Floor Planning
- To understand FPGA based system: Basic concept, Digital Design Digital Design and FPGA, FPGA Fabrics: FPGA architecture and its description Static RAM based FPGA, Permanent FPGA, Chip I/O, Circuit design of FPGA, Logic implementation of FPGA architecture

COURSE OUTCOMES (CO):

After completion of the course, a student will be able to

COURSE OUTCOME (CO)	DESCRIPTION
CO1	Acquire basic knowledge on the Architecture of 8051 µc
CO2	Analyze Data path logic cell, Sequential logic cell, I/O cell, cell compiler.
CO3	Develop analysis capability in Programmable ASIC Design, Anti fuse, Static RAM, EPROM, EEPROM Technology
CO4	Develop competence in Low level Design Entry, Schematic design Entry
CO5	Identify functions of FPGA architecture

CO-PO MAPPING:

	CO	PO1 Engineering Knowledge	PO2 Problem Analysis	PO3 Design/development of solutions	PO4 Conduct investigations into complex problems	PO5 Modern tool usage	PO6 Engineer and Society	PO7 Environment and Sustainability	PO8 Ethics	PO9 Individual and Team work	PO10 Communication	PO11 Project Management and Finance	PO12 Lifelong learning
CO1	Acquire basic knowledge on the working of Architecture of 8051 µc	**3**											**1**
CO2	Analyze Data path logic cell, Sequential logic cell, I/O cell, cell compiler	**3**		**2**									**1**
CO3	Develop analysis capability in Programmable ASIC Design, Anti fuse, Static RAM, EPROM, EEPROM Technology	**3**		**2**		**2**							
CO4	Develop competence in Low level Design Entry, Schematic design Entry	**3**		**1**									
CO5	Identify functions of FPGA architecture. .	**3**											**2**
3: Strong contribution, 2: average contribution, 1: Low contribution													

SYLLABUS WITH CO:

UNIT	CONTENT	CO
I	Introduction to embedded system design, Design issue in system development, Architecture of 8051 µc and its description, Pin diagram of 8051 µc and its description, addressing modes, instruction sets, Arithmetic and logical operation, Sub-router, Interrupt handling timing sub-router, Serial data transmission, Serial data communication	**1**
II	Introduction to ASIC, Types of ASIC, ASIC cell library, CMOS logic, CMOS Process, CMOS Design rule, Combinational logics, Combinational logics, Data path logic cell, Sequential logic cell, I/O cell, cell compiler	**2**
III	ASIC library cell design: Transistor and resistors, Transistor parasitic capacitance, Logical Effort, Library cell design, Library architecture, Gate array design, standard cell design, Programmable ASIC Design, Anti fuse, Static RAM, EPROM, EEPROM Technology	**3**
IV	Low level Design Entry, Schematic design Entry, Language, PLA, Tool, EDIF, Overview, Hardware descriptive language VHDL, Hardware descriptive language Verilog, Logic synthesis VHDL Simulation, Logic synthesis VHDL Simulation, Floor Planning	**4**
V	FPGA based system: Basic concept, Digital Design Digital Design and FPGA, FPGA Fabrics: FPGA architecture and its description Static RAM based FPGA, Permanent FPGA, Chip I/O, Circuit design of FPGA, Logic implementation of FPGA architecture	**5**

RECOMMENDED BOOKS:

Text Books:

1. M J S Smith/ Application Specific Integration Circuit. Pearson Edu 2005

Reference Books:

1. K J Ayla/ 8051 microcontroller/ paperback 3rd Edition 2005

INTEGRAL UNIVERSITY, LUCKNOW
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

COURSE: Semiconductor Device Modeling & Circuits Simulation (DC)
COURSE CODE: EC 501
COURSE CREDIT: 4

PREREQUISITES:

Subject	Description	Level of study
Electronics Devices & Circuits.	Basic understanding of various semiconductor devices and circuits.	Undergraduate
VLSI Design	Concept of layout design, Elements of device electronics.	Undergraduate

COURSE OBJECTIVES:

- Basic understanding of various semiconductor devices and modeling of circuits.
- To introduce the students to the knowledge of modeling and simulation of BJT and MOS circuits.
- To examine the basic building blocks of large-scale digital integrated circuits.

COURSE OUTCOMES (CO):

After completion of the course, a student will be able to learn

COURSE OUTCOME (CO)	DESCRIPTION
CO1	Compound semiconductors, Lattice structures, Carrier drift, Direct and indirect semiconductors Scattering, Recombination, Mean life time, Continuity equation.
CO2	PN junction characteristics, Current components in diode, Equivalent circuits of diode, BJT characteristics, Second order effects in BJT: Thermal runaway, Base width modulation, Kirk effect, Band gap narrowing, Small signal analysis.
CO3	Eber's moll model, Hybrid pi model, Figure of merit, approximate model and complete equivalent model of BJT, Charge control model, Gummel poon model, SPICE model of BJT, Simulation of BJT.
CO4	N-channel, P-channel MOS characteristics and features, Enhancement and depletion mode: second order effects of MOS: Body effect, Channel length modulation, Subthreshold conduction, DIBL, Hot carrier effect, Mobility degradation, Velocity saturation, CMOS latch up, MOS parasitic capacitances and resistances.
CO5	Circuits models for MOSFET: small signal, SPICE models, BSIM model, Simulation and Layout design DC, AC and Transient analysis of linear and non linear circuits, logic and timing simulations.

CO-PO MAPPING:

	CO	PO1 Engineering Knowledge	PO2 Critical Thinking	PO3 Problem Solving	PO4 Research Skill	PO5 Usage of modern tool usage	PO6 Collaborative and Multidisciplinary work	PO7 Project Management and Finance	PO8 Communication	PO9 Life-long Learning	PO10 Ethical Practices and Social Responsibility	PO11 Independent and Reflective Learning
CO1	Compound semiconductors, Lattice structures, Carrier drift, Direct and indirect semiconductors Scattering, Recombination, Mean life time, Continuity equation	**3**	**2**	**3**	**1**				**1**	**2**		
CO2	PN junction characteristics, Current components in diode, Equivalent circuits of diode, BJT characteristics, Second order effects in BJT: Thermal runaway, Base width modulation, Kirk effect, Band gap narrowing, Small signal analysis.	**3**	**2**	**2**	**1**				**2**		**1**	

CO3	Eber's moll model, Hybrid pi model, Figure of merit, approximate model and complete equivalent model of BJT, Charge control model, Gummel poon model, SPICE model of BJT, Simulation of BJT		**3**	**3**	**2**	**3**				**2**	**1**	
CO4	N-channel, P-channel MOS characteristics and features, Enhancement and depletion mode: second order effects of MOS: Body effect, Channel length modulation, Subthreshold conduction, DIBL, Hot carrier effect, Mobility degradation, Velocity saturation, CMOS latch up, MOS parasitic capacitances and resistances.	**3**	**2**	**1**	**2**	**3**				**2**	**2**	

CO5	Circuits models for MOSFET: small signal, SPICE models, BSIM model, Simulation and Layout design DC, AC and Transient analysis of linear and non linear circuits, logic and timing simulations.	**3**	**2**	**1**	**1**	**3**				**1**	**2**	

SYLLABUS WITH CO:

UNIT	CONTENT	CO
I	Compound semiconductors, Lattice structures, Carrier drift, Direct and indirect semiconductors Scattering, Recombination, Mean life time, Continuity equation	**1**
II	PN junction characteristics, Current components in diode, Equivalent circuits of diode, BJT characteristics, Second order effects in BJT: Thermal runaway, Base width modulation, Kirk effect, Band gap narrowing, Small signal analysis.	**2**
III	Eber's moll model, Hybrid pi model, Figure of merit, approximate model and complete equivalent model of BJT, Charge control model, Gummel poon model, SPICE model of BJT, Simulation of BJT	**3**
IV	N-channel, P-channel MOS characteristics and features, Enhancement and depletion mode: second order effects of MOS: Body effect, Channel length modulation, Subthreshold conduction, DIBL, Hot carrier effect, Mobility degradation, Velocity saturation, CMOS latch up, MOS parasitic capacitances and resistances.	**4**
V	Circuits models for MOSFET: small signal, SPICE models, BSIM model, Simulation and Layout design DC, AC and Transient analysis of linear and non linear circuits, logic and timing simulations.	**5**

Text Books:

1. Baker, Li, Boyce " CMOS Layout, Design and simulation", PHI publication
2. Rabaey Jan M, Chandrakasan Anantha, Nikolic Borivoje " Digital Integrated Circuits" PHI publication
3. Kanno Kannan " Semiconductor Devices and Physics" Wiley publication
4. Sze S.M. " Semiconductor Physics" MacGraw Hill publication

Reference Books:

1. Millman, Halkias " Electronic Devices and Circuits" TMH publication
2. Kamins Muller " Device Electronics for Integrated Circuis" Wiley publication

INTEGRAL UNIVERSITY, LUCKNOW
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

COURSE: Device Modeling & Circuits Simulation (DC)
COURSE CODE: EC 505
COURSE CREDIT: 1

PREREQUISITES:
Circuit Simulation Lab and VLSI Design Lab
CO-REQUISITES
Semiconductor Device Modeling & Circuits Simulation (DC)

COURSE OBJECTIVES:

- To introduce the students to the knowledge of modeling and simulation of BJT and MOS circuits.
- To examine the basic building blocks of large-scale digital integrated circuits.

COURSE OUTCOMES (CO):

After completion of the course, a student will be able to learn

COURSE OUTCOME (CO)	DESCRIPTION
CO1	To study and design a depletion load NMOS inverter with given specifications also analyze its characteristics..
CO2	To study and design a symmetrical CMOS inverter for a given data and calculate VM for VTC, noise margin, Plot VTC with and without body effect and design a parallel CMOS Inverter.
CO3	To study and design a CMOS inverter delay with specified limitation and design a two i/p CMOS NAND inverter with its plots.
CO4	To design a current mirror using CMOS technology also analyze its characteristics.

CO-PO MAPPING:

	CO	PO1 Engineering Knowledge	PO2 Critical Thinking	PO3 Problem Solving	PO4 Research Skill	PO5 Usage of modern tool usage	PO6 Collaborative and Multidisciplinary work	PO7 Project Management and Finance	PO8 Communication	PO9 Life-long Learning	PO10 Ethical Practices and Social Responsibility	PO11 Independent and Reflective Learning
CO1	To study and design a depletion load NMOS inverter with given specifications also analyze its characteristics..	**3**	**2**	**3**	**1**				**1**	**2**		
CO2	To study and design a symmetrical CMOS inverter for a given data and calculate VM for VTC, noise margin, Plot VTC with and without body effect and design a parallel CMOS Inverter.	**3**	**2**	**2**	**1**				**2**		**1**	
CO3	To study and design a CMOS inverter delay with specified limitation and design a two i/p CMOS NAND inverter with its plots.		**3**	**3**	**2**	**3**				**2**	**1**	
CO4	To design a current mirror using CMOS technologies also analyze its characteristics.	**3**	**2**	**1**	**2**	**3**				**2**	**2**	

INTEGRAL UNIVERSITY, LUCKNOW
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

COURSE: Digital System Design using Verilog HDL
COURSE CODE: EC 504
COURSE CREDIT: 4

PREREQUISITES:

Subject	Description	Level of study
Digital Electronics	Boolean Algebra , Combinational and Sequential circuit, Memory	B.Tech.

COURSE OBJECTIVES:

- Improve the student background and basic knowledge in the fields of HDL programming.
- Improve the student skills in the logical design of digital systems.
- To explain combinational ,sequential circuits and Concept of PLA and PLDs.
- To explain the verilog HDL with detailed study of structural data flow and behavioral modeling.
- To explain the test bench and simulation of combinational and sequential circuits
- To Study of RTL Coding Guidelines, Modelsim Simulation Tool, Synthesis Tool, Synplify Tool, Xilinx Place & Route Tool.
- Design of Memories – ROM, RAM , Design of Arithmetic Circuits, System Design,

COURSE OUTCOMES (CO):

COURSE OUTCOME (CO)	DESCRIPTION
CO1	Student will be able to understand the concept of VLSI Design flow and will able design the combinational circuit using PLDs and PAL.
CO2	Student will able design the sequential circuit i.e. different types of registers and counters etc. Student will be able to understand the concept of Design Flow of VLSI Circuits
CO3	Student will be able to explain HDL languages and its type .Student will able to design combinational and sequential circuit using structural modeling, dataflow modeling and behavioral modeling of Verilog HDL
CO4	Student will able to write the test bench of digital circuits. Student will able to design system using ASM Chart , able to work on Modelsim and will able to simulate the combinational and sequential circuit on it.
CO5	Student will able to design the ROM , RAM , arithmetic circuits and system like ATM machine , weighing machine etc. using Verilog HDL.

CO-PO MAPPING:

	CO	**PO1** Engineering Knowledge	**PO2** Critical Thinking	**PO3** Problem Solving	**PO4** Research Skill	**PO5** Usage of modern tool usage	**PO6** Collaborative and Multidisciplinary work	**PO7** Project Management and Finance	**PO8** Communication	**PO9** Life-long Learning	**PO10** Ethical Practices and Social Responsibility	**PO11** Independent and Reflective Learning
CO1	Student will be able to understand the concept of VLSI Design flow and will able design the combinational circuit using PLDs and PAL.	**3**	**3**	**3**	**1**					**2**		**1**
CO2	Student will able design the sequential circuit i.e. different types of registers and counters etc. Student will be able to understand the concept of Design Flow of VLSI Circuits.	**3**	**3**	**3**	**1**					**2**		**2**
CO3	Student will be able to explain HDL languages and its type .Student will able to design combinational and sequential circuit using structural modeling, dataflow modeling and behavioral modeling of Verilog HDL	**3**	**3**	**3**	**3**	**3**		**2**	**2**	**2**		**2**
CO4	Student will able to write the test bench of digital circuits. Student will able to design system using ASM Chart , able to work on Modelsim and will able to simulate the combinational and sequential circuit on it.	**3**	**3**	**3**	**3**	**3**		**2**	**2**	**2**	**2**	**2**
CO5	Student will able to design the ROM , RAM , arithmetic circuits and system like ATM machine , weighing machine etc. using Verilog HDL.	**3**	**3**	**3**	**3**	**3**	**1**	**3**	**3**	**2**	**2**	**2**

SYLLABUS WITH CO:

UNIT	CONTENT	CO
I	Introduction to VLSI Design, Combinational Circuit Design, Programmable Logic Devices, Programmable Array Logic.	**1**
II	Review of Flip-Flops, Sequential Circuits, Sequential Circuit Design, Design Flow of VLSI Circuits.	**2**
III	Verilog Modeling of Combinational Circuits, Modeling of Verilog Sequential Circuits, RTL Coding Guidelines, Coding Organization - Complete Realization.	**3**
IV	Writing a Test Bench, System Design using ASM Chart, Example of System Design using ASM Chart, Examples of System Design using Sequential Circuits, Simulation of Combinational and Sequential Circuits, Analysis of Waveforms using Modelsim.	**4**
V	Model Sim Simulation Tool, Synthesis Tool, Synplify Tool - Schematic Circuit Diagram View, Xilinx Place & Route Tool, Design of Memories – ROM, RAM , Design of Arithmetic Circuits, System Design Examples.	**5**

RECOMMENDED BOOKS:

Text Book:

1. Samir Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", PHI.

Reference Books:

1. "John F Wakerley,"Digital Design Principles and Practice", PHI

INTEGRAL UNIVERSITY, LUCKNOW
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

COURSE: ANALOG MOS CIRCUITS
COURSE CODE: EC507
COURSE CREDIT: 4

PREREQUISITES:

Subject	Description	Level of study
None	**None**	-

COURSE OBJECTIVES:

- To learn about differential amplifier and single stage MOS amplifiers.
- To understand different types of MOS current mirrors and frequency response.
- To tell the concept of feedback in MOS circuits and noise.
- To teach about oscillators and PLL.
- To impart knowledge of operational amplifiers and switched capacitor circuits.

COURSE OUTCOMES (CO):
After completion of the course, a student will be able to

COURSE OUTCOME (CO)	DESCRIPTION
CO1	Students will **know** about different topologies of single stage MOS amplifiers. Students will able to **understand** the concept of differential amplifiers.
CO2	Student shall be able to **learn** and **understand** about MOS current mirrors and frequency response of circuits.
CO3	Students shall able to **know** about noise in MOS circuits. Students will also learn about feedback and their different topologies.
CO4	Student will **know** about different oscillator circuits their operation. Students will **learn** about phase lock loop
CO5	Student shall be able to **know** about operational amplifier and their property. Students will **learn** about switched capacitor circuits and their applications as amplifiers, filters, integrators and ADC/DAC

CO-PO MAPPING:

	CO	**PO1** Engineering Knowledge	**PO2** Problem Analysis	**PO3** Design/development of solutions	**PO4** Conduct investigations into complex problems	**PO5** Modern tool usage	**PO6** Engineer and Society	**PO7** Environment and Sustainability	**PO8** Ethics	**PO9** Individual and Team work	**PO10** Communication	**PO11** Project Management and Finance	**PO12** Lifelong learning
CO1	Students will **know** about different topologies of single stage MOS amplifiers. Students will able to **understand** the concept of differential amplifiers.	**3**	**3**	**3**	**2**	**2**	**1**		**1**	**2**			**1**
CO2	Student shall be able to **learn** and **understand** about MOS current mirrors and frequency response of circuits.	**3**	**3**	**3**	**3**	**3**	**1**			**1**			**1**
CO3	Students shall able to **know** about noise in MOS circuits. Students will also learn about feedback and their different topologies.	**3**	**3**	**3**	**3**	**2**	**2**			**2**			**1**
CO4	Student will **know** about different oscillator circuits their operation. Students will **learn** about phase lock loop	**3**	**3**	**3**	**3**	**2**	**1**			**1**			**1**
CO5	Student shall be able to **know** about operational amplifier and their property. Students will **learn** about switched capacitor circuits and their applications as amplifiers, filters, integrators and ADC/DAC	**3**	**2**	**3**	**2**	**2**	**2**			**2**			**1**
3: Strong contribution, 2: average contribution, 1: Low contribution													

SYLLABUS WITH CO:

UNIT	CONTENT	CO
I	Single Stage MOS Amplifiers: Common source stage with resistive load, Diode connected load and Source degeneration, Source follower, Common gate stage, Cascode stage Differential Amplifiers: Quantitative and qualitative analysis of basic differential amplifier, Common mode response, Differential pair with MOS Loads	**1**
II	MOS Current Mirrors: Basic current mirrors, Cascode current mirrors, Active current mirrors Frequency Response of Amplifiers: Miller effect, Poles and zeroes, Analysis of CS, CD, CG stage, Cascode stage and Differential pair	**2**
III	Noise: Statistical Characteristics of Noise, Thermal noise, Flicker noise, Representation of noise in circuits, Noise in CS, CD, CG stage, Cascode stage and Differential pair Feedback: Properties of Feedback, Feedback topologies, Effect of loading in Feedback, Effect of feedback on noise	**3**
IV	Oscillators: Oscillation criterion, Ring Oscillators, LC oscillators, Voltage controlled oscillators Phase-Locked Loop: Simple PLL, Charge-Pump PLL, Delay locked loop	**4**
V	Operational Amplifiers: Performance parameters, One stage and two stage Op-Amps, Gain boosting, Common mode feedback, Slew rate, Power supply rejection, Noise in Op-Amp, Stability and Frequency compensation in Op-Amp Switched Capacitor Circuits: MOS as a switch, Different switched capacitors circuits, Applications as Amplifiers, Filters, Integrators and ADC/DAC	**5**

RECOMMENDED BOOKS:

Text Books:

1. Razavi Behzad ”Design of analog CMOS Integrated Circuits” Tata McGraw-Hill Edition, 2002

INTEGRAL UNIVERSITY, LUCKNOW
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

COURSE: ***VLSI DEVICES & CIRCUITS***
COURSE CODE: EC502
COURSE CREDIT: 4

PREREQUISITES:

Subject	Description	Level of study
None	**None**	-

COURSE OBJECTIVES:

- To learn about properties of digital systems, scaling and small geometry effects.
- To understand different types of standard CMOS circuits and PTL.
- To tell the concept of dynamic and domino CMOS circuits.
- To teach about different standard cell and circuit implementation using PAL and PLA, FPGA.
- To impart knowledge of different types of memories.

COURSE OUTCOMES (CO):

After completion of the course, a student will be able to

COURSE OUTCOME (CO)	DESCRIPTION
CO1	Students will **know** about properties of digital systems. Students will able to **understand** the concept of scaling and short channel effects.
CO2	Students shall able to **know** about standard CMOS logic and pass transistor logic. Students will also learn about design and sizing of MOSFETs.
CO3	Student shall be able to **learn** and **understand** about dynamic and domino logic design.
CO4	Student will **know** about standard cells. Students will **learn** circuit implementation using PAL and PLA, FPGA
CO5	Student shall be able to **know** about different memory circuits and their operation. Students will also learn about BiCMOS and GaAs MESFET.

CO-PO MAPPING:

	CO	**PO1** Engineering Knowledge	**PO2** Problem Analysis	**PO3** Design/development of solutions	**PO4** Conduct investigations into complex problems	**PO5** Modern tool usage	**PO6** Engineer and Society	**PO7** Environment and Sustainability	**PO8** Ethics	**PO9** Individual and Team work	**PO10** Communication	**PO11** Project Management and Finance	**PO12** Lifelong learning
CO1	Students will **know** about properties of digital systems. Students will able to **understand** the concept of scaling and short channel effects.	**3**	**3**	**3**	**2**	**1**	**1**		**1**	**2**			**1**
CO2	Students shall able to **know** about standard CMOS logic and pass transistor logic. Students will also learn about design and sizing of MOSFETs.	**3**	**3**	**3**	**3**	**2**	**1**			**2**			**1**
CO3	Student shall be able to **learn** and **understand** about dynamic and domino logic design.	**3**	**3**	**2**	**3**	**2**	**1**			**1**			**1**
CO4	Student will **know** about standard cells. Students will **learn** circuit implementation using PAL and PLA, FPGA	**3**	**3**	**3**	**3**	**2**	**1**			**1**			**1**
CO5	Student shall be able to **know** about different memory circuits and their operation. Students will also learn about BiCMOS and GaAs MESFET.	**3**	**3**	**2**	**2**	**2**	**1**			**1**			**1**
3: Strong contribution, 2: average contribution, 1: Low contribution													

SYLLABUS WITH CO:

UNIT	CONTENT	CO
I	Properties of digital systems, regenerative property, NMOS, PMOS, pull up and pull down networks, strong 1 and strong 0, NAND/NOR, EX-OR, Decoder, MUX,Micron and Sub-micron devices: Scaling, Short channel effects	**1**
II	Standard CMOS circuits, Pseudo NMOS, Pass Transistor Logic (PTL), types of PTL, advantages and disadvantages of PTL, Level restorer, Transmission gate Adder/ Substractor, Design of Combinational circuits & Sizing of MOSFETs	**2**
III	Dynamic CMOS and Domino CMOS, Complex gates, Sequential Circuits: Latches & Flip-flops, Problems of race, race around and 1's catching	**3**
IV	Standard cells, Circuit implementation using PAL and PLA, FPGA, Look up tables (LUTs), Importance of FPGA	**4**
V	RAM, ROM, basic cells of SRAM and DRAM, 6T RAM, 3T RAM, 1T RAM, GaAs MESFET, its characteristics and applications, Bi-CMOS: features, inverter, conventional and full swing BiCMOS circuits	**5**

RECOMMENDED BOOKS:

Text Books:

1. Rabaey Jan M, Chandrakasan Anantha, Nikolic Borivoje " Digital Integrated Circuits" PHI publication
2. Hodges, Jackson, Saleh " Analysis and Design of Digital Integrated Circuits" McGraw Hill publication
3. Kang Sung-Mo, Leblebici Yusuf "CMOS Digital Integrated Circuits" Tata McGraw Hill publication

Reference Books:

1. Sedra ,Smith " Microelectronic Circuits" Oxford Publication
2. Islam S.S "Semiconductor Devices and Physics" Oxford Publication

INTEGRAL UNIVERSITY LUCKNOW
Faculty of Engineering
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

M.Tech. Electronics Circuits & Systems

M.Tech ECS II[nd] Yr Semester: IV[th]	**ECE-509 Fault Modeling and Testing of Electronic Circuits**	L T P C 3 1 0 4

Course Objectives:

- To understand the basic concepts of semiconductor physics and Fundamentals of silicon crystal structures, orientation planes and their effects and also nature and effects of impurities like carbon, oxygen etc.
- To understand the concepts of Yield, Yield loss, failure and models of failure analysis, Gate level testing and their fault models, chip level testing and their fault models.
- To understand the concept behind the five valued logic, truth table generation of standard gates, Boolean algebra, its use and testing, introduction to Stuck-at faults.
- To understand the concept of CMOS test methods, Functionality and manufacturing test principles, ATPG, Fault grading, delay fault testing, Statical fault analysis design strategies.
- To understand the concept of Functional testing, Ad-hoc scan-based testing, self-testing and IDDQ Testing, also Chip level & system level testing examples.

Course Outcome (CO)

CO.1	**Understand** the silicon crystal structures**. Identify** the orientation plane and explain their effects and also nature and effects of impurities like carbon, oxygen etc. To **apply** the basics of Parametric problems and effects in fabrication, also know the circuit sensitivities.
CO.2	**Analyze** Yield, Yield loss, failure and models of failure analysis. **Explain** the Gate level testing and their fault models. chip level testing and their fault models.
CO.3	**Design** and **analyze** of five valued logics **Describe** the application of truth table generation of standard gates, Boolean algebra its use in testing. Also to **describe** the Stuck-at faults.
CO.4	**List** and **explain** the different CMOS test methods. **TO understand** Functionality and manufacturing test principles, ATPG, Fault grading, delay fault testing, Statical fault analysis design strategies.
CO.5	**To understand** the concept of Functional testing, Ad-hoc scan-based testing, self-testing. **Differentiate** between Chip level & system level testing examples.

Unit	Course Contents:	Mapped CO	hours
I	Fundamentals of silicon crystal structures, orientation planes and their effects, nature and effects of impurities like carbon, oxygen etc., Parametric problems and effects in fabrication, circuit sensitivities	**CO.1**	**8**
II	Yield, Yield loss, failure and models of failure analysis, Gate level testing and their fault models, chip level testing and their fault models	**CO.2**	**8**
III	Introduction to five valued logic, truth table generation of standard gates, Boolean algebra, its use and testing, Stuck-at faults	**CO.3**	**8**

Signature HoD	*Approval Date*	Revision effective from 2016-2017

IV	CMOS test methods, Functionality and manufacturing test principles, ATPG, Fault grading, delay fault testing, Statical fault analysis design strategies	**CO.4**	**8**
V	Functional testing, Ad-hoc scan-based testing, self-testing and IDDQ Testing, Chip level & system level testing examples	**CO.5**	**8**

References (Text Books):

1. Lala P.K."Fault Tolerant and Fault Testable Hardware Design" BS Publication
2. Sze S.M. "VLSI Technology" TMH Publication
3. Weste Neil H.E., Eshraghian Kamran "Principle of CMOS VLSI Design" 2nd ed Pearson
4. Hurst Stanley Leonard "VLSI Testing" IEEE Circuits and Devices Series

Course Articulation Matrix: (Mapping of COs with POs and PSOs)

PO-PSO	PO												PSO			
CO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**	**PSO3**	**PSO4**
CO1	3	3	2	1	1	1		1	1			3	2	3	2	1
CO2	3	3	3	3	3	1			1			1	3	3	2	
CO3	3	3	2	3	3	1			1			1	3	3	1	
CO4	3	3	3	2	2				1			1	3	2	2	
CO5	3	3	2	3	3				2			1	3	2	2	

1- Low Correlation; 2- Moderate Correlation; 3- Substantial Correlation

INTEGRAL UNIVERSITY, LUCKNOW
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

COURSE: RF Circuit Design & Technology
COURSE CODE: EC 601
COURSE CREDIT: 4

PREREQUISITES:

Subject	Description	Level of study
Integrated Circuit	Review of Basic Integrated Circuits, Multipliers	B.Tech. III Year

COURSE OBJECTIVES:

- To understand the RF and wireless technology, spectrum allocation, can identify issues in the design of RF circuits, can apply Maximum RF power transfer theorem.
- To learn the basic building blocks in RF systems-RF transmitters and receivers. Can understand the basic low noise amplifier design and the oscillator, mixer design and input & output characteristics of RF amplifier.
- To learn the analysis of the transistor equivalent circuit-Y parameters, S parameters, the MOS transistor biasing-design using Y parameters, MOS transistor biasing-design using S parameters and power amplifier design.
- To understand the concept and design of sheet resistance, skin effect, parasitic capacitance, parasitic inductance and diffusion resistors.
- To understand the concepts of inductors and transformers.

COURSE OUTCOMES (CO):

After completion of the course, a student will be able to

COURSE OUTCOME (CO)	DESCRIPTION
CO1	Students shall be able to understand RF and wireless technology, spectrum allocation, identify issues in the design of RF circuits, apply maximum RF power transfer theorem.
CO2	For a given RF system, student shall be able to analyze basic building blocks in RF systems-RF transmitters and receivers and evaluate the low noise amplifier design and predict the oscillator, mixer design and input & output characteristics of RF amplifier.
CO3	For a given RF system, student shall be able to analyze the transistor equivalent circuit-Y parameters, S parameters. Examine and analyze the MOS transistor biasing-design using Y parameters, MOS transistor biasing-design using S parameters and power amplifier design.
CO4	Students shall be able to identify the technology back end and metallization in IC technologies and will be able to understand sheet resistance, skin effect, parasitic capacitance, parasitic inductance and diffusion resistors.
CO5	For a given a RF system, student shall be able to design the inductors and transformers and will be able to understand the self-resonance of inductors, the quality factor of an inductor, characterization of an inductor, layout of spiral inductors, isolating the Inductor, the use of slotted ground shields. Analyze the basic transformer layouts in IC technologies and radio architectures of GSM, CDMA and UMTS.

CO-PO MAPPING:

	CO	**PO1** Engineering Knowledge	**PO2** Critical Thinking	**PO3** Problem Solving	**PO4** Research Skill	**PO5** Usage of modern tool usage	**PO6** Collaborative and Multidisciplinary work	**PO7** Project Management and Finance	**PO8** Communication	**PO9** Life-long Learning	**PO10** Ethical Practices and Social Responsibility	**PO11** Independent and Reflective Learning
CO1	Students shall be able to understand RF and wireless technology, spectrum allocation, identify issues in the design of RF circuits, apply maximum RF power transfer theorem.	**3**	**2**						**1**			
CO2	For a given RF system, student shall be able to analyze basic building blocks in RF systems-RF transmitters and receivers and evaluate the low noise amplifier design and predict the oscillator, mixer design and input & output characteristics of RF amplifier.	**3**	**2**									
CO3	For a given RF system, student shall be able to analyze the transistor equivalent circuit-Y parameters, S parameters. Examine and analyze the MOS transistor biasing-design using Y parameters, MOS transistor biasing-design using S parameters and power amplifier design.	**3**	**3**	**3**	**2**	**1**						
CO4	Students shall be able to identify the technology back end and metallization in IC technologies and will be able to understand sheet resistance, skin effect, parasitic capacitance, parasitic inductance and diffusion resistors.	**3**	**2**	**1**	**2**							
CO5	For a given a RF system, student shall be able to design the inductors and transformers and will be able to understand the self-resonance of inductors, the quality factor of an inductor, characterization of an inductor, layout of spiral inductors, isolating the Inductor, the use of slotted ground shields. Analyze the basic transformer layouts in IC technologies and radio architectures of GSM, CDMA and UMTS.	**3**	**2**	**1**	**1**	**1**				**1**		

SYLLABUS WITH CO:

UNIT	CONTENT	CO
I	**Introduction:** Introduction to RF and wireless technology, spectrum allocation, issues in the design of RF circuits, PCB, Electronic chips, Transmission media and reflections, Maximum RF power transfer, Applications of RF.	**1**
II	**RF circuit design:** Basic building blocks in RF systems – RF Transmitters and receivers, Antenna, impedance matching, Noise, Low noise amplifier design and Linearity, Oscillator, Mixer design, Filter design, Input & output characteristics of RF Amplifier, Nonlinearity and time variance, Inter-symbol interference, Random process and noise, Sensitivity and dynamic range, Passive impedance transformation; Issues in RFIC Design.	**2**
III	The Transistor Equivalent Circuit – Y Parameters, S Parameters, Understanding RF transistor data sheets, MOS Transistor Biasing - Design Using Y Parameters, MOS Transistor Biasing - Design Using S Parameters, RF Power Transistor Characteristics - Transistor Biasing, Power Amplifier Design - Matching to Coaxial Feed lines, Automatic Shutdown Circuitry, Broadband Transformers	**3**
IV	The Technology Back End and Metallization in IC Technologies, Sheet Resistance and the Skin Effect, Parasitic Capacitance, Parasitic Inductance, Current Handling in Metal Lines, Poly Resistors and Diffusion Resistors, Metal-Insulator-Metal Capacitors, Poly Capacitors.	**4**
V	Applications of On-Chip Spiral Inductors and Transformers, Design of Inductors and Transformers, Some Basic Lumped Models for Inductors, Calculating the Inductance of Spirals, Self-Resonance of Inductors, The Quality Factor of an Inductor, Characterization of an Inductor, Layout of Spiral Inductors, Isolating the Inductor, The Use of Slotted Ground Shields and Inductors, Basic Transformer Layouts in IC Technologies, Multilevel Inductors, Characterizing Transformers for Use in ICs, On-Chip Transmission Lines, Effect of Transmission Line, Transmission, High High-Frequency Measurement of On-Chip, Passives, Some Common De-Embedding Techniques, radio architectures of GSM, CDMA and UMTS.	**5**

RECOMMENDED BOOKS:

Text Book:

1. RF circuit design by Chris Bowick , Elsevier's Science & Technology Rights Department in Oxford, UK.
2. RF Microelectronics by Behzard Razavi, Prentice Hall Ptr.
3. Radio Frequency Integrated Circuit Design, John Rogers, Calvin Plett, Artech House.
4. The RF and microwave handbook, CRC Press.
5. The RF transmission systems Edited by Jerr y C. Whitaker, CRC Press.

Reference Books:

1. "Fundamentals of Logic Design", Charles H. Roth, Jr., 5th Edition, Brooks/Cole, a division of Thomson, 2004.
2. "Digital Principles and Application", D P Leach, A P Malvino and Goutam Saha, 7th Edition, TMH
3. "Digital Design - Principles and Practices" , J F Wakerly, 4th Edition, Pearson Education.